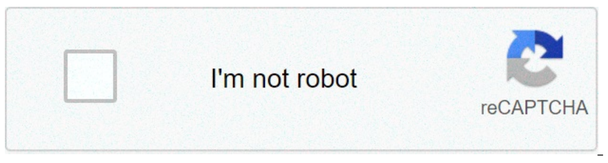

Continue

The operation of a jfet involves

[ENGN2211 Home] A schematic representation of an n channel JFET is shown in Figure 118. An n-type channel is formed between two p-type layers which are connected to the gate. Majority carrier electrons flow from the source and exit the drain, forming the drain current. The pn junction is reverse biased during normal operation, and this widens the depletion layers which extend into the n channel only (since the doping of the p regions is much larger than that of the n channel). As the depletion layers widen, the channel narrows, restricting current flow. Figure 118: n-channel JFET structure. When , there is little voltage drop along the length of the channel, and the depletion regions are parallel, Figure 119. As vGS is increased negatively, they eventually touch reducing iD to zero. The value of vGS at which this occurs is called the pinch-off voltage, Vp (or vGS(off)). Figure: n-channel JFET structure for showing parallel depletion regions. When , there is a voltage drop along the length of the channel, and the depletion regions are no longer parallel, but are closer together towards the drain, Figure 120. As vDS is increased, they will touch (pinch-off) towards the drain, and the drain current iD can increase no longer. At the threshold of pinch-off, vGS-vDS=Vp. As vDS is further increased, iD remains constant, and the JFET is in its current saturation region, the normal mode of operation. (This constant current region is a characteristic feature of any transistor, FET or BJT.) The channel shape remains unchanged, with a small region of touch near the drain, and further increases in vDS occurs across this small region. Figure: n-channel JFET structure for showing non-parallel depletion regions. JFETS are high input impedance devices, and so (due to the reverse bias pn junctions). [ENGN2211 Home] ANU Engineering - ENGN2211 Voltage sweeps are a great way to learn about the device. Figure \(\PageIndex{10}\) shows a typical plot of drain-source voltage sweeps at various gate-source voltages while measuring the drain current, ID for a n-channel JFET. The V-I characteristics have four distinct regions. Analysis of these regions can provides critical information about the device characteristics such as the pinch off voltage, VP, transcunductance gain, gm, drain-source channel resistance, RDS, and power dissipation, PD. Figure adapted from Electronic Tutorials (www.electronic-tutorials.ws). This region is bounded by VDS < VP. Here the JFET begins to flow a drain current with a linear response to the voltage, behaving like a variable resistor. In this region the drain-source channel resistance, RDS is modeled by \ref{1}, where ΔVDS is the change in drain-source voltage, ΔID is the change in drain current, and gm is the transcunductance gain. Solving for gm results in \ref{2}. \[R_{DS}\ =\ \frac{\Delta V_{DS}}{\Delta I_{D}}\ =\ \frac{1}{g_{m}} \label{1} \] \[g_m\ =\ \frac{\Delta I_{D}}{\Delta V_{DS}}\ =\ \frac{1}{R_{DS}} \label{2} \] This is the region where the JFET is completely "ON". The maximum amount of current is flowing for the given gate-source voltage. In this region the drain current can be modeled by the \ref{3}, where ID is the drain current, IDSS is the maximum current, VGS is the gate-source voltage, and VP is the pinch off voltage. Solving for the pinch off voltage results in \ref{4}. \[I_{D}\ =\ I_{DSS}(1\ -\ \frac{V_{GS}}{V_{P}}) \label{3} \] \[V_{P}\ =\ 1\ -\ \frac{V_{GS}}{\sqrt{\frac{I_D}{I_{DSS}}}} \label{4} \] This region is characterized by the sudden increase in current. The drain-source voltage supplied exceeds the resistive limit of the semiconducting channel, resulting in the transistor to break down and flow an uncontrolled current. In this region the gate-source voltage is sufficient to restrict the flow through the channel, in effect cutting off the drain current. The power dissipation, PD, can be solved utilizing Ohms law (I = V/R) for any region using \ref{5}. \[P_{D}\ =\ I_{D}\ \times \ V_{DC}\ =\ (I_{D})^{2}\ \times \ R_{DS}\ =\ (V_{DS})^{2}/R_{DS} \label{5} \] The p-channel JFET V-I characteristics behave similarly except that the voltages are reversed. Specifically, the pinch off point is reached when the gate-source voltage is increased in a positive direction, and the saturation region is met when the drain-source voltage is increased in the negative direction. Figure \(\PageIndex{11}\) shows a typical plot of drain-source voltage sweeps at various gate-source voltages while measuring the drain current, ID for an ideal n-channel enhancement MOSFET. Like JFETs, the V-I characteristics of MOSFETS have distinct regions that provide valuable information about device transport properties. Figure adapted from Electronic Tutorials (www.electronic-tutorials.ws). The n-channel enhanced MOSFET behaves linearly, acting like a variable resistor, when the gate-source voltage is greater than the threshold voltage and the drain-source voltage is greater than the gate-source voltage. In this region the drain current can be modeled by \ref{6}, where ID is the drain current, VGS is the gate-source voltage, VT is the threshold voltage, VDS is the drain-source voltage, and k is the geometric factor described by \ref{7}, where µn is the charge-carrier effective mobility, COX is the gate oxide capacitance, W is the channel width, and L is the channel length. \[I_{D}\ =\ 2k((V_{GS}-V_{T})V_{DS}\ -\ [(V_{DS})^{2}/2]} \label{6} \] \[k\ =\ \mu _{n} C_{OX} \frac{W}{L} \label{7} \] In this region the MOSFET is considered fully "ON". The drain current for the saturation region is modeled by \ref{8}. The drain current is mainly influenced by the gate-source voltage, while the drain-source voltage has no effect. \[I_{D}\ =\ k(V_{GS}\ -\ V_{T})^{2} \label{8} \] Solving for the threshold voltage VT results in \ref{9}. \[V_{T}\ =\ V_{GS}\ -\ \sqrt{\frac{I_{D}}{k}} \label{9} \] When the gate-source voltage, VGS, is below the threshold voltage VT the charge carriers in the channel are not available "cutting off" the charge flow. Power dissipation for MOSFETs can also be solved using equation 6 in any region as in the JFET case. The typical I-V characteristics for the whole family of FETs seen in Figure \(\PageIndex{11}\) are plotted in Figure \(\PageIndex{12}\). Figure \(\PageIndex{12}\) Plot of V-I characteristics for the various FET types. Adapted from P. Horowitz and W. Hill, in Art of Electronics, Cambridge University Press, New York, 2nd Edn., 1994. From Figure \(\PageIndex{12}\) we can see how the doping schemes that lead to enhancement and depletion are displaced along the VGS axis. In addition, from the plot the ON or OFF state can be determined for a given gate-source voltage, where (+) is positive, (0) is zero, and (-) is negative, as seen in Table \(\PageIndex{1}\). Table \(\PageIndex{1}\): The ON/OFF state for the various FETs at a given gate-source voltages where (-) is a negative voltage and (+) is a positive voltage. FET Type VGS = (-) VGS = 0 VGS = (+) n-channel JFET OFF ON ON p-channel JFET ON ON OFF n-channel depletion MOSFET OFF ON ON p-channel depletion MOSFET ON ON OFF n-channel enhancement MOSFET OFF OFF ON p-channel enhancement MOSFET ON ON OFF 21. For a JFET, if the gate voltage VGS is made more negative, then the channel conductivity increases depletion region increases channel conductivity decreases channel current increases 22. The main drawbacks of a JFET is its high input impedance low input impedance higher noise lower gain 23. A field effect transistor (FET) has three pn junction uses a forward-biased junction depends on the variation of a reverse voltage for its operation depends on the variation of magnetic field for its operation 24. The operation of a JFET involves a flow of minority carriers a flow of majority carriers recombination negative resistance 25. What is the range of a FET's input impedance? 10 Ω to 1 kΩ 1 kΩ to 10 kΩ 50 kΩ to 100 kΩ 1 MΩ to 100 MΩ 26. A FET is a better chopper than a BJT because it has lower offset voltage higher series ON resistance lower input current higher input impedance 27. In a N-channel JFET, drain current is maximum when gate voltage VGS is equal to +VDD more than to + VDD equal to '0' volts all the above 28. Which of the following is a common feature of FET? They have high input impedance These are voltage-controlled devices They have isolated input and output all of these 29. FET belongs to which of the following type of device? current-controlled device magnetic device power controlled device voltage-controlled device 30. The control parameter of JFET is gate current drain voltage gate voltage source voltage 31. The transit time of the current carriers through the channel of a FET decides its ___________ characteristics. switching on/off dynamic load 32. As compared to FET, BJT has _________ input impedance and _________ output impedance. low, low low, high high, high high, low 33. The following statements refer to an n channel FET operated in the active region: the gate voltage VGS reverse biases the junction. The drain voltage VDD is negative with respect to the source. the current in the n channel is due to electrons. increasing the reverse bias VGS increases the cross section for conduction. Which of these statements are correct? i and ii i and iii ii and iii iii and iv 34. Compared to the bipolar junction transistor, a JFET has a larger gain bandwidth produce is less noisy has less input resistance has current flow due to only majority carriers i, ii, iii and iv are correct i and ii are correct ii and iv are correct iii and iv are correct 35. Thermal runaway is not encountered in FETs because IDS has a zero temperature coefficient IDS has a negative temperature coefficient IDS has a positive temperature coefficient the mobility of the carriers increases with increase in temperature 36. A JFET is set up as a follower, with µ = 200, rd = 100 kΩ and source load resistor RL = 1 kΩ. The output resistance Ro is 37. Consider following statements: BJT is a current controlled device with high input impedance and high gain bandwidth FET is a voltage controlled device with high input impedance and low gain bandwidth UJT is a negative resistance device and can be used as an oscillator BJT, FET and UJT can all be used for amplification. Which of these statements are correct? i and ii ii and iii iii and iv i and iv "FET" redirects here. For other uses, see FET (disambiguation). Type of transistor Cross-sectional view of a field-effect transistor, showing source, gate and drain terminals The field-effect transistor (FET) is a type of transistor that uses an electric field to control the flow of current. FETs are devices with three terminals: source, gate, and drain. FETs control the flow of current by the application of a voltage to the gate, which in turn alters the conductivity between the drain and source. FETs are also known as unipolar transistors since they involve single-carrier-type operation. That is, FETs use either electrons or holes as charge carriers in their operation, but not both. Many different types of field effect transistors exist. Field effect transistors generally display very high input impedance at low frequencies. The most widely used field-effect transistor is the MOSFET (metal-oxide-semiconductor field-effect transistor). History Further information: History of the transistor Julius Edgar Lilienfeld proposed the concept of a field-effect transistor in 1925. The concept of a field-effect transistor (FET) was first patented by Austro-Hungarian physicist Julius Edgar Lilienfeld in 1925[1] and by Oskar Heil in 1934, but they were unable to build a working practical semiconducting device based on the concept. The transistor effect was later observed and explained by John Bardeen and Walter Houser Brattain while working under William Shockley at Bell Labs in 1947, shortly after the 17-year patent expired. Shockley initially attempted to build a working FET, by trying to modulate the conductivity of a semiconductor, but was unsuccessful, mainly due to problems with the surface states, the dangling bond, and the germanium and copper compound materials. In the course of trying to understand the mysterious reasons behind their failure to build a working FET, it led to Bardeen and Brattain instead inventing the point-contact transistor in 1947, which was followed by Shockley's bipolar junction transistor in 1948.[2][3] The first FET device to be successfully built was the junction field-effect transistor (JFET).[2] A JFET was first patented by Heinrich Welker in 1945.[4] The static induction transistor (SIT), a type of JFET with a short channel, was invented by Japanese engineers Jun-ichi Nishizawa and Y. Watanabe in 1950. Following Shockley's theoretical treatment on the JFET in 1952, a working practical JFET was built by George F. Dacey and Ian M. Ross in 1953.[5] However, the JFET still had issues affecting junction transistors in general.[6] Junction transistors were relatively bulky devices that were difficult to manufacture on a mass-production basis, which limited them to a number of specialised applications. The insulated-gate field-effect transistor (IGFET) was theorized as a potential alternative to junction transistors, but researchers were unable to build working IGFETs, largely due to the troublesome surface state barrier that prevented the external electric field from penetrating into the material.[6] By the mid-1950s, researchers had largely given up on the FET concept, and instead focused on bipolar junction transistor (BJT) technology.[7] The foundations of MOSFET technology were laid down by the work of William Shockley, John Bardeen and Walter Brattain. Shockley independently envisioned the FET concept in 1945, but he was unable to build a working device. The next year Bardeen explained his failure in terms of surface states. Bardeen applied the theory of surface states on semiconductors (previous work on surface states was done by Shockley in 1939 and Igor Tamm in 1932) and realized that the external field was blocked at the surface because of extra electrons which are drawn to the semiconductor surface. Electrons become trapped in those localized states forming an inversion layer. Bardeen's hypothesis marked the birth of surface physics. Bardeen then decided to make use of an inversion layer instead of the very thin layer of semiconductor which Shockley had envisioned in his FET designs. Based on his theory, in 1948 Bardeen patented the progenitor of MOSFET, an insulated-gate FET (IGFET) with an inversion layer. The inversion layer confines the flow of minority carriers, increasing modulation and conductivity, although its electron transport depends on the gate's insulator or quality of oxide if used as an insulator, deposited above the inversion layer. Bardeen's patent as well as the concept of an inversion layer forms the basis of CMOS technology today. In 1976 Shockley described Bardeen's surface state hypothesis "as one of the most significant research ideas in the semiconductor program".[8] After Bardeen's surface state theory the trio tried to overcome the effect of surface states. In late 1947, Robert Gibney and Brattain suggested the use of electrolyte placed between metal and semiconductor to overcome the effects of surface states. Their FET device worked, but amplification was poor. Bardeen went further and suggested to rather focus on the conductivity of the inversion layer. Further experiments led them to replace electrolyte with a solid oxide layer in the hope of getting better results. Their goal was to penetrate the oxide layer and get to the inversion layer. However, Bardeen suggested they switch from silicon to germanium and in the process their oxide got inadvertently washed off. They stumbled upon a completely different transistor, the point-contact transistor. Lillian Hoddeson argues that "had Brattain and Bardeen been working with silicon instead of germanium they would have stumbled across a successful field effect transistor".[8][9][10][11][12] By the end of the first half of the 1950s, following theoretical and experimental work of Bardeen, Brattain, Kingston, Morrison and others, it became more clear that there were two types of surface states. Fast surface states were found to be associated with the bulk and a semiconductor/oxide interface. Slow surface states were found to be associated with the oxide layer because of adsorption of atoms, molecules and ions by the oxide from the ambient. The latter were found to be much more numerous and to have much longer relaxation times. At the time Philo Farnsworth and others came up with various methods of producing atomically clean semiconductor surfaces. In 1955, Carl Frosch and Lincoln Derrick accidentally covered the surface of silicon wafer with a layer of silicon dioxide. They showed that oxide layer prevented certain dopants into the silicon wafer, while allowing for others, thus discovering the passivating effect of oxidation on the semiconductor surface. Their further work demonstrated how to etch small openings in the oxide layer to diffuse dopants into selected areas of the silicon wafer. In 1957, they published a research paper and patented their technique summarizing their work. The technique they developed is known as oxide diffusion masking, which would later be used in the fabrication of MOSFET devices. At Bell Labs, the importance of Frosch's technique was immediately realized. Results of their work circulated around Bell Labs in the form of BTL memos before being published in 1957. At Shockley Semiconductor, Shockley had circulated the preprint of their article in December 1956 to all his senior staff, including Jean Hoerni.[6][13][14] In 1955, Ian Munro Ross filed a patent for a FeFET or MFSFET. Its structure was like that of a modern inversion channel MOSFET, but ferroelectric material was used as a dielectric/insulator instead of oxide. He envisioned it as a form of memory, years before the floating gate MOSFET. In February 1957, John Wallmark filed a patent for FET in which germanium monoxide was used as a gate dielectric, but he didn't pursue the idea. In his other patent filed the same year he described a double gate FET. In March 1957, in his laboratory notebook, Ernesto Labate, a research scientist at Bell Labs, conceived of a device similar to the later proposed MOSFET, although Labate's device didn't explicitly use silicon dioxide as an insulator.[15][16][17][18] Metal-oxide-semiconductor FET (MOSFET) Main article: MOSFET Mohamed Atalla (left) and Dawon Kahng (right) invented the MOSFET (MOS field-effect transistor) in 1959. A breakthrough in FET research came with the work of Egyptian engineer Mohamed Atalla in the late 1950s.[3] In 1958 he presented experimental work which showed that growing thin silicon oxide on clean silicon surface leads to neutralization of surface states. This is known as surface passivation, a method that became critical to the semiconductor industry as it made mass-production of silicon integrated circuits possible.[19][20] The metal–oxide–semiconductor field-effect transistor (MOSFET) was then invented by Mohamed Atalla and Dawon Kahng in 1959.[21][22] The MOSFET largely superseded both the bipolar transistor and the JFET,[2] and had a profound effect on digital electronic development.[23][22] With its high scalability,[24] and much lower power consumption and higher density than bipolar junction transistors,[25] the MOSFET made it possible to build high-density integrated circuits.[26] The MOSFET is also capable of handling higher power than the JFET.[27] The MOSFET was the first truly compact transistor that could be miniaturised and mass-produced for a wide range of uses.[6] The MOSFET thus became the most common type of transistor in computers, electronics,[20] and communications technology (such as smartphones).[28] The US Patent and Trademark Office calls it a "groundbreaking invention that transformed life and culture around the world".[28] CMOS (complementary MOS), a semiconductor device fabrication process for MOSFETs, was developed by Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor in 1963.[29][30] The first report of a floating-gate MOSFET was made by Dawon Kahng and Simon Sze in 1967.[31] A double-gate MOSFET was first demonstrated in 1984 by Electrotechnical Laboratory researchers Toshihiro Sekigawa and Yutaka Hayashi.[32][33] FinFET (fin field-effect transistor), a type of 3D non-planar multi-gate MOSFET, originated from the research of Digh Hisamoto and his team at Hitachi Central Research Laboratory in 1989.[34][35] Basic information See also: Charge carrier § Majority and minority carriers FETs can be majority-charge-carrier devices, in which the current is carried predominantly by majority carriers, or minority-charge-carrier devices, in which the current is mainly due to a flow of minority carriers.[36] The device consists of an active channel through which charge carriers, electrons or holes, flow from the source to the drain. Source and drain terminal conductors are connected to the semiconductor through ohmic contacts. The conductivity of the channel is a function of the potential applied across the gate and source terminals. The FET's three terminals are:[37] source (S), through which the carriers enter the channel. Conventionally, current entering the channel at S is designated by IS. drain (D), through which the carriers leave the channel. Conventionally, current entering the channel at D is designated by ID. Drain-to-source voltage is VDS. gate (G), the terminal that modulates the channel conductivity. By applying voltage to G, one can control ID. More about terminals Cross section of an n-type MOSFET All FETs have source, drain, and gate terminals that correspond roughly to the emitter, collector, and base of BJTs. Most FETs have a fourth terminal called the body, base, bulk, or substrate. This fourth terminal serves to bias the transistor into operation; it is rare to make non-trivial use of the body terminal in circuit designs, but its presence is important when setting up the physical layout of an integrated circuit. The size of the gate, length L in the diagram, is the distance between source and drain. The width is the extension of the transistor, in the direction perpendicular to the cross section in the diagram (i.e., into/out of the screen). Typically the width is much larger than the length of the gate. A gate length of 1 µm limits the upper frequency to about 5 GHz, 0.2 µm to about 30 GHz. The names of the terminals refer to their functions. The gate terminal may be thought of as controlling the opening and closing of a physical gate. This gate permits electrons to flow through or blocks their passage by creating or eliminating a channel between the source and drain. Electron-flow from the source terminal towards the drain terminal is influenced by an applied voltage. The body simply refers to the bulk of the semiconductor in which the gate, source and drain lie. Usually the body terminal is connected to the highest or lowest voltage within the circuit, depending on the type of the FET. The body terminal and the source terminal are sometimes connected together since the source is often connected to the highest or lowest voltage within the circuit, although there are several uses of FETs which do not have such a configuration, such as transmission gates and cascode circuits. Effect of gate voltage on current I–V characteristics and output plot of a JFET n-channel transistor. Simulation result for right side: formation of inversion channel (electron density) and left side: current-gate voltage curve (transfer characteristics) in an n-channel nanowire MOSFET. Note that the threshold voltage for this device lies around 0.45 V. FET conventional symbol types The FET controls the flow of electrons (or electron holes) from the source to drain by affecting the size and shape of a "conductive channel" created and influenced by voltage (or lack of voltage) applied across the gate and source terminals. (For simplicity, this discussion assumes that the body and source are connected.) This conductive channel is the "stream" through which electrons flow from source to drain. n-channel FET In an n-channel "depletion-mode" device, a negative gate-to-source voltage causes a depletion region to expand in width and encroach on the channel from the sides, narrowing the channel. If the active region expands to completely close the channel, the resistance of the channel from source to drain becomes large, and the FET is effectively turned off like a switch (see right figure, when there is very small current). This is called "pinch-off", and the voltage at which it occurs is called the "pinch-off voltage". Conversely, a positive gate-to-source voltage increases the channel size and allows electrons to flow easily (see right figure, when there is a conduction channel and current is large). In an n-channel "enhancement-mode" device, a conductive channel does not exist naturally within the transistor, and a positive gate-to-source voltage is necessary to create one. The positive voltage attracts free-floating electrons within the body towards the gate, forming a conductive channel. But first, enough electrons must be attracted near the gate to counter the dopant ions added to the body of the FET; this forms a region with no mobile carriers called a depletion region, and the voltage at which this occurs is referred to as the threshold voltage of the FET. Further gate-to-source voltage increase will attract even more electrons towards the gate which are able to create a conductive channel from source to drain; this process is called inversion. p-channel FET In a p-channel "depletion-mode" device, a positive voltage from gate to body widens the depletion layer by forcing electrons to the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, positively charged acceptor ions. Conversely, in a p-channel "enhancement-mode" device, a conductive region does not exist and negative voltage must be used to generate a conduction channel. Effect of drain-to-source voltage on channel For either enhancement- or depletion-mode devices, at drain-to-source voltages much less than gate-to-source voltages, changing the gate voltage will alter the channel resistance, and drain current will be proportional to drain voltage (referenced to source voltage). In this mode the FET operates like a variable resistor and the FET is said to be operating in a linear mode or ohmic mode.[38][39] If drain-to-source voltage is increased, this creates a significant asymmetrical change in the shape of the channel due to a gradient of voltage potential from source to drain. The shape of the inversion region becomes "pinched-off" near the drain end of the channel. If drain-to-source voltage is increased further, the pinch-off point of the channel begins to move away from the drain towards the source. The FET is said to be in saturation mode;[40] although some authors refer to it as active mode, for a better analogy with bipolar transistor operating regions.[41][42] The saturation mode, or the region between ohmic and saturation, is used when amplification is needed. The in-between region is sometimes considered to be part of the ohmic or linear region, even where drain current is not approximately linear with drain voltage. Even though the conductive channel formed by gate-to-source voltage no longer connects source to drain during saturation mode, carriers are not blocked from flowing. Considering again an n-channel enhancement-mode device, a depletion region exists in the p-type body, surrounding the conductive channel and drain and source regions. The electrons which comprise the channel are free to move out of the channel through the depletion region if attracted to the drain by drain-to-source voltage. The depletion region is free of carriers and has a resistance similar to silicon. Any increase of the drain-to-source voltage will increase the distance from drain to the pinch-off point, increasing the resistance of the depletion region in proportion to the drain-to-source voltage applied. This proportional change causes the drain-to-source current to remain relatively fixed, independent of changes to the drain-to-source voltage, quite unlike its ohmic behavior in the linear mode of operation. Thus, in saturation mode, the FET behaves as a constant-current source rather than as a resistor, and can effectively be used as a voltage amplifier. In this case, the gate-to-source voltage determines the level of constant current through the channel. Composition FETs can be constructed from various semiconductors—silicon is by far the most common. Most FETs are made by using conventional bulk semiconductor processing techniques, using a single crystal semiconductor wafer as the active region, or channel. Among the more unusual body materials are amorphous silicon, polycrystalline silicon or other amorphous semiconductors in thin-film transistors or organic field-effect transistors (OFETs) that are based on organic semiconductors; often, OFET gate insulators and electrodes are made of organic materials, as well. Such FETs are manufactured using a variety of materials such as silicon carbide (SiC), gallium arsenide (GaAs), gallium nitride (GaN), and indium gallium arsenide (InGaAs). In June 2011, IBM announced that it had successfully used graphene-based FETs in an integrated circuit.[43][44] These transistors are capable of about 2.23 GHz cutoff frequency, much higher than standard silicon FETs.[45] Types Depletion-type FETs under typical voltages: JFET, poly-silicon MOSFET, double-gate MOSFET, metal-gate MOSFET, MESFET. Depletion Electrons Holes Metal Insulator Top: source, bottom: drain, left: gate, right: bulk. Voltages that lead to channel formation are not shown. The channel of a FET is doped to produce either an n-type semiconductor or a p-type semiconductor. The drain and source may be doped of opposite type to the channel, in the case of enhancement mode FETs, or doped of similar type to the channel as in depletion mode FETs. Field-effect transistors are also distinguished by the method of insulation between channel and gate. Types of FETs include: The MOSFET (metal–oxide–semiconductor field-effect transistor) utilizes an insulator (typically SiO2) between the gate and the body. This is by far the most common type of FET. The DGMOSFET (dual-gate MOSFET) or DGMOS, a MOSFET with two insulated gates. The IGBT (insulated-gate bipolar transistor) is a device for power control. It has a structure akin to a MOSFET coupled with a bipolar-like main conduction channel. These are commonly used for the 200–3000 V drain-to-source voltage range of operation. Power MOSFETs are still the device of choice for drain-to-source voltages of 1 to 200 V. The MNOS (metal–nitride–oxide–semiconductor transistor) utilizes a nitride-oxide layer insulator between the gate and the body. The ISFET (ion-sensitive field-effect transistor) can be used to measure ion concentrations in a solution; when the ion concentration (such as H+, see pH electrode) changes, the current through the transistor will change accordingly. The BioFET (Biologically sensitive field-effect transistor) is a class of sensors/biosensors based on ISFET technology which are utilized to detect charged molecules; when a charged molecule is present, changes in the electrostatic field at the BioFET surface result in a measurable change in current through the transistor. These include enzyme modified FETs (EnFETs), immunologically modified FETs (ImmunoFETs), gene-modified FETs (GenFETs), DNAFETs, cell-based BioFETs (CPFETs), beetle/chip FETs (BeetleFETs), and FETs based on ion-channels/protein binding.[46] The DNAFET (DNA field-effect transistor) is a specialized FET that acts as a biosensor, by using a gate made of single-strand DNA molecules to detect matching DNA strands. The JFET (junction field-effect transistor) uses a reverse biased p–n junction to separate the gate from the body. The static induction transistor (SIT) is a type of JFET with a short channel. The DEPFET is a FET formed in a fully depleted substrate and acts as a sensor, amplifier and memory node at the same time. It can be used as an image (photon) sensor. The FREDFET (fast-reverse or fast-recovery epitaxial diode FET) is a specialized FET designed to provide a very fast recovery (turn-off) of the body diode, making it convenient for driving inductive loads such as electric motors, especially medium-powered brushless DC motors. The HIGFET (heterostructure insulated-gate field-effect transistor) is now used mainly in research.[47] The MODFET (modulation-doped field-effect transistor) is a high-electron-mobility transistor using a quantum well structure formed by graded doping of the active region. The TFET (tunnel field-effect transistor) is based on band-to-band tunneling.[48] The HEMT (high-electron-mobility transistor), also called a HFET (heterostructure FET), can be made using bandgap engineering in a ternary semiconductor such as AlGaAs. The fully depleted wide-band-gap material forms the isolation between gate and body. The MESFET (metal–semiconductor field-effect transistor) substitutes the p–n junction of the JFET with a Schottky barrier; and is used in GaAs and other III-V semiconductor materials. The NOMFET is a nanoparticle organic memory field-effect transistor.[49] The GNRFET (graphene nanoribbon field-effect transistor) uses a graphene nanoribbon for its channel.[50] The VeSFET (vertical-slit field-effect transistor) is a square-shaped junctionless FET with a narrow slit connecting the source and drain at opposite corners. Two gates occupy the other corners, and control the current through the slit.[51] The CNTFET (carbon nanotube field-effect transistor). The OFET (organic field-effect transistor) uses an organic semiconductor in its channel. The QFET (quantum field effect transistor) takes advantage of quantum tunneling to greatly increase the speed of transistor operation by eliminating the traditional transistor's area of electron conduction. The SB-FET (Schottky-barrier field-effect transistor) is a field-effect transistor with metallic source and drain contact electrodes, which create Schottky barriers at both the source-channel and drain-channel interfaces.[52][53] The GFET is a highly sensitive graphene-based field effect transistor used as biosensors and chemical sensors. Due to the 2 dimensional structure of graphene, along with its physical properties, GFETs offer increased sensitivity, and reduced instances of 'false positives' in sensing applications[54] The Fe FET uses a ferroelectric between the gate, allowing the transistor to retain its state in the absence of bias - such devices may have application as non-volatile memory. Advantages The FET has high gate-to-drain current resistance, on the order of 100 MΩ or more, providing a high degree of isolation between control and flow. Because base current noise will increase with shaping time,[55] a FET typically produces less noise than a bipolar junction transistor (BJT), and is found in noise-sensitive electronics such as tuners and low-noise amplifiers for VHF and satellite receivers. It is relatively immune to radiation. It exhibits no offset voltage at zero drain current and makes an excellent signal chopper. It typically has better thermal stability than a BJT.[37] Because they are controlled by gate charge, once the gate is closed or open, there is no additional power draw, as there would be with a bipolar junction transistor or with non-latching relays in some states. This allows extremely low-power switching, which in turn allows greater miniaturization of circuits because heat dissipation needs are reduced compared to other types of switches. Disadvantages A field-effect transistor has a relatively low gain–bandwidth product compared to a BJT. The MOSFET is very susceptible to overload voltages, thus requiring special handling during installation.[56] The fragile insulating layer of the MOSFET between the gate and channel makes it vulnerable to electrostatic discharge or changes to threshold voltage during handling. This is not usually a problem after the device has been installed in a properly designed circuit. FETs often have a very low "on" resistance and have a high "off" resistance. However, the intermediate resistances are significant, and so FETs can dissipate large amounts of power while switching. Thus efficiency can put a premium on switching quickly, but this can cause transients that can excite stray inductances and generate significant voltages that can couple to the gate and cause unintentional switching. FET circuits can therefore require very careful layout and can involve trades between switching speed and power dissipation. There is also a trade-off between voltage rating and "on" resistance, so high-voltage FETs have a relatively high "on" resistance and hence conduction losses.[citation needed] Failure modes FETs are relatively robust, especially when operated within the temperature and electrical limitations defined by the manufacturer (proper derating). However, modern FET devices can often incorporate a body diode. If the characteristics of the body diode are not taken into consideration, the FET can experience slow body diode behavior, where a parasitic transistor will turn on and allow high current to be drawn from drain to source when the FET is off.[57] Uses This section does not cite any sources. Please help improve this section by adding citations to reliable sources. Unsourced material may be challenged and removed. (September 2018) (Learn how and when to remove this template message) The most commonly used FET is the MOSFET. The CMOS (complementary metal oxide semiconductor) process technology is the basis for modern digital integrated circuits. This process technology uses an arrangement where the (usually "enhancement-mode") p-channel MOSFET and n-channel MOSFET are connected in series such that when one is on, the other is off. In FETs, electrons can flow in either direction through the channel when operated in the linear mode. The naming convention of drain terminal and source terminal is somewhat arbitrary, as the devices are typically (but not always) built symmetrical from source to drain. This makes FETs suitable for switching analog signals between paths (multiplexing). With this concept, one can construct a solid-state mixing board, for example. FET is commonly used as an amplifier. For example, due to its large input resistance and low output resistance, it is effective as a buffer in common-drain (source follower) configuration. IGBTs are used in switching internal combustion engine ignition coils, where fast switching and voltage blocking capabilities are important. Source-gated transistor Source-gated transistors are more robust to manufacturing and environmental issues in large-area electronics such as display screens, but are slower in operation than FETs.[58] See also Chemical field-effect transistor CMOS FET amplifier FinFET FlowFET Multigate device References ^ Lilienfeld, J.E. "Method and apparatus for controlling electric current" US Patent no. 1,745,175 (filed: 8 October 1926 ; issued: 28 January 1930). ^ a b c Lee, Thomas H. (2003). The Design of CMOS Radio-Frequency Integrated Circuits (PDF). Cambridge University Press. ISBN 9781139643771. ^ a b Puers, Robert; Baldi, Livio; Voorde, Marcel Van de; Nooten, Sebastiaan E. van (2017). Nanoelectronics: Materials, Devices, Applications, 2 Volumes. John Wiley & Sons. p. 14. ISBN 9783527340538. ^ Grundmann, Marius (2010). The Physics of Semiconductors. Springer-Verlag. ISBN 978-3-642-13884-3. ^ Jun-Ichi Nishizawa (1982). "Junction Field-Effect Devices". Semiconductor Devices for Power Conditioning. Springer. pp. 241–272. doi:10.1007/978-1-4684-7263-9_11. ISBN 978-1-4684-7265-3. Missing or empty |title= (help) ^ a b c d Moskowitz, Sanford L. (2016). Advanced Materials Innovation: Managing Global Technology in the 21st century. John Wiley & Sons. p. 168. ISBN 9780470508923. ^ "The Foundation of Today's Digital World: The Triumph of the MOS Transistor". Computer History Museum. 13 July 2010. Retrieved 21 July 2019. ^ a b Howard R. Duff (2001). "John Bardeen and transistor physics". AIP Conference Proceedings. 550. pp. 3–32. doi:10.1063/1.1354371. ^ Hans Camenzind (2005). Designing Analog Chips. ^ ULSI Science and Technology/1997. 1997. p. 43. ISBN 9781566771306. ^ Lillian Hoddeson (1994). "Research on crystal rectifiers during World War II and the invention of the transistor". History and Technology. 11 (2): 121–130. doi:10.1080/07341519408581858. ^ Michael Riordan, Lillian Hoddeson (1997). Crystal Fire: The Birth of the Information Age. ISBN 9780393041248.CS1 maint: uses authors parameter (link) ^ Christophe Lécuyer; David C. Brook; Jay Last (2010). Makers of the Microchip: A Documentary History of Fairchild Semiconductor. pp. 62–63. ISBN 978-0262014243.CS1 maint: uses authors parameter (link) ^ Claeys, Cor L. (2003). ULSI Process Integration III: Proceedings of the International Symposium. The Electrochemical Society. pp. 27–30. ISBN 978-1566773768. ^ Lojek, Bo (2007). History of Semiconductor Engineering. Springer Science & Business Media. p. 324. ISBN 978-3540342588. ^ Stefan Ferdinand Müller (2016). Development of HfO2-Based Ferroelectric Memories for Future CMOS Technology Nodes. ISBN 9783739248943. ^ B.G Lowe; R.A. Sareen (2013). Semiconductor X-Ray Detectors. ISBN 9781466554016.CS1 maint: uses authors parameter (link) ^ Bassett, Ross Knox (2007). To the Digital Age: Research Labs, Start-up Companies, and the Rise of MOS Technology. Johns Hopkins University Press. p. 22. ISBN 978-0801886393. ^ "Martin Atalla in Inventors Hall of Fame, 2009". Retrieved 21 June 2013. ^ a b "Dawon Kahng". National Inventors Hall of Fame. Retrieved 27 June 2019. ^ "1960 - Metal Oxide Semiconductor (MOS) Transistor Demonstrated". The Silicon Engine. Computer History Museum. ^ a b Lojek, Bo (2007). History of Semiconductor Engineering. Springer Science & Business Media. pp. 321–3. ISBN 9783540342588. ^ "960 - Metal Oxide Semiconductor (MOS) Transistor Demonstrated". The Silicon Engine. Computer History Museum. ^ Motoyoshi, M. (2009). "Through-Silicon Via (TSV)". Proceedings of the IEEE. 97 (1): 43–48. doi:10.1109/JPROC.2008.2007462. ISSN 0018-9219. S2CID 29105721. ^ "Transistors Keep Moore's Law Alive". EETimes. 12 December 2018. Retrieved 18 July 2019. ^ "Who Invented the Transistor?". Computer History Museum. 4 December 2013. Retrieved 20 July 2019. ^ Duncan, Ben (1996). High Performance Audio Power Amplifiers. Elsevier. p. 177. ISBN 9780080508047. ^ a b "Remarks by Director Iancu at the 2019 International Intellectual Property Conference". United States Patent and Trademark Office. June 10, 2019. Retrieved 20 July 2019. ^ "1963: Complementary MOS Circuit Configuration is Invented". Computer History Museum. Retrieved 6 July 2019. ^ U.S. Patent 3,102,230, filed in 1960, issued in 1963 ^ D. Kahng and S. M. Sze, "A floating gate and its application to memory devices", The Bell System Technical Journal, vol. 46, no. 4, 1967, pp. 1288–1295 ^ Colinge, J.P. (2008). FinFETs and Other Multi-Gate Transistors. Springer Science & Business Media. p. 11. ISBN 9780387717517. ^ Sekigawa, Toshihiro; Hayashi, Yutaka (1 August 1984). "Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate". Solid-State Electronics. 27 (8): 827–828. doi:10.1016/0038-1101(84)90036-4. ISSN 0038-1101. ^ "IEEE Andrew S. Grove Award Recipients". IEEE Andrew S. Grove Award. Institute of Electrical and Electronics Engineers. Retrieved 4 July 2019. ^ "The Breakthrough Advantage for FPGAs with Tri-Gate Technology" (PDF). Intel. 2014. Retrieved 4 July 2019. ^ Jacob Millman (1985). Electronic devices and circuits. Singapore: McGraw-Hill International. p. 397. ISBN 978-0-07-085505-2. ^ a b Jacob Millman (1985). Electronic devices and circuits. Singapore: McGraw-Hill. pp. 384–385. ISBN 978-0-07-085505-2. ^ Galup-Montoro, C.; Schneider, M.C. (2007). MOSFET modeling for circuit analysis and design. London/Singapore: World Scientific. p. 83. ISBN 978-981-256-810-6. ^ Norbert R Malik (1995). Electronic circuits: analysis, simulation, and design. Englewood Cliffs, NJ: Prentice Hall. pp. 315–316. ISBN 978-0-02-374910-0. ^ Spencer, R.R.; Ghausi, M.S. (2001). Microelectronic circuits. Upper Saddle River NJ: Pearson Education/Prentice-Hall. p. 102. ISBN 978-0-201-36183-4. ^ Sedra, A. S.; Smith, K.C. (2004). Microelectronic circuits (Fifth ed.). New York: Oxford University Press. p. 552. ISBN 978-0-19-514251-8. ^ PR Gray; PJ Hurst; SH Lewis; RG Meyer (2001). Analysis and design of analog integrated circuits (Fourth ed.). New York: Wiley. pp. §1.5.2 p. 45. ISBN 978-0-471-32168-2. ^ Bob Yirka (10 January 2011). "IBM creates first graphene based integrated circuit". Phys.org. Retrieved 14 January 2019. ^ Lin, Y.-M.; Valdes-Garcia, A.; Han, S.-J.; Farmer, D. B.; Sun, Y.; Wu, Y.; Dimitrakopoulos, C.; Grill, A; Avouris, P; Jenkins, K. A. (2011). "Wafer-Scale Graphene Integrated Circuit". Science. 332 (6035): 1294–1297. doi:10.1126/science.1204428. PMID 21659599. S2CID 3020496. ^ Belle Dumé (10 December 2012). "Flexible graphene transistor sets new records". Physics World. Retrieved 14 January 2019. ^ Schöning, Michael J.; Poghossian, Arshak (2002). "Recent advances in biologically sensitive field-effect transistors (BioFETs)" (PDF). Analyst. 127 (9): 1137–1151. doi:10.1039/B204444G. PMID 12375833. ^ freepatentsonline.com, HIGFET and method - Motorola] ^ Ionescu, A. M.; Riel, H. (2011). "Tunnel field-effect transistors as energy-efficient electronic switches". Nature. 479 (7373): 329–337. doi:10.1038/nature10679. PMID 22094693. S2CID 4322368. ^ "Organic transistor paves way for new generations of neuro-inspired computers". ScienceDaily. January 29, 2010. Retrieved January 14, 2019. ^ Sarvari H.; Ghayour, R.; Dastjerdy, E. (2011). "Frequency analysis of graphene nanoribbon FET by Non-Equilibrium Green's Function in mode space". Physica E: Low-dimensional Systems and Nanostructures. 43 (8): 1509–1513. doi:10.1016/j.physe.2011.04.018. ^ Jerzy Ruzyllo (2016). Semiconductor Glossary: A Resource for Semiconductor Community. World Scientific. p. 244. ISBN 978-981-4749-56-5. ^ Appenzeller, J, et al. (November 2008). "Toward Nanowire Electronics". IEEE Transactions on Electron Devices. 55 (11): 2827–2845. doi:10.1109/ted.2008.2008011. ISSN 0018-9383. OCLC 755663637. S2CID 703393. ^ Prakash, Abhijith; Ilatikhameneh, Hesameddin; Wu, Peng; Appenzeller, Joerg (2017). "Understanding contact gating in Schottky barrier transistors from 2D channels". Scientific Reports. 7 (1): 12596. doi:10.1038/s41598-017-12816-3. ISSN 2045-2322. OCLC 1010581463. PMC 5626721. PMID 28974712. ^ Miklos, Bolza. "What Are Graphene Field Effect Transistors (GFETs)?". Graphenea. Retrieved 14 January 2019. ^ VIII.5. Noise in Transistors ^ Allen Mottershead (2004). Electronic devices and siraj circuits. New Delhi: Prentice-Hall of India. ISBN 978-81-203-0124-5. ^ Slow Body Diode Failures of Field Effect Transistors (FETs): A Case Study. ^ Sporea, R.A.; Trainor, M.J.; Young, N.D.; Silva, S.R.P. (2014). "Source-gated transistors for order-of-magnitude performance improvements in thin-film digital circuits". Scientific Reports. 4: 4295. doi:10.1038/srep04295. PMC 3944386. PMID 24599023. External links Wikimedia Commons has media related to Field-effect Transistors. PBS The Field Effect Transistor How Semiconductors and Transistors Work (MOSFETs) WeCanFigureThisOut.org Junction Field Effect Transistor CMOS gate circuitry Winning the Battle Against Latchup in CMOS Analog Switches Field Effect Transistors in Theory and Practice The Field Effect Transistor as a Voltage Controlled Resistor "The FET (field effect transistor)". rolinychupetin (L.R.Linares). March 30, 2013 – via YouTube. Retrieved from "